What is claimed is:

1. A conducting interface device comprising:

a contact opening in a dielectric layer on a semiconductor substrate;

an alloy material formed on the semiconductor substrate and within the contact opening in the dielectric layer;

a continuous barrier metal formed within the contact opening in the dielectric layer, formed over and adjoining walls of the contact opening and the alloy material; and

a first contact material formed over the barrier metal.

2. The conducting interface device of claim 1, further comprising a transistor source/drain region in the semiconductor substrate wherein the contact opening opens to at least a portion of the transistor source/drain region.

3. The conducting interface device of claim 1, wherein the alloy material includes silicon and germanium.

4. The conducting interface device of claim 1, wherein the alloy material is formed on the semiconductor substrate and within the contact opening by epitaxial deposition.

5. The conducting interface device of claim 1, wherein the barrier metal includes:

a layer of titanium (Ti); and

a layer of titanium nitride (TiN) coupled to the layer of titanium (Ti).

6. The conducting interface device of claim 1, wherein the first contact material includes aluminum.

7. A conducting interface device comprising:

a contact opening in a dielectric layer on a semiconductor substrate;

an oxide layer on the dielectric layer, and within the contact opening in the dielectric layer; and

an alloy material coupled to the semiconductor substrate and coupled to the oxide layer within the contact opening.

8. The conducting interface device of claim 7, wherein the oxide layer includes tetraethyl orthosilicate (TEOS).

9. The conducting interface device of claim 7, wherein the dielectric layer includes borophosphorus silicate glass (BPSG).

10. The conducting interface device of claim 7, wherein the semiconductor substrate includes silicon.

11. The conducting interface device of claim 7, wherein the alloy material includes silicon and germanium.

12. A conducting interface device comprising:

a contact opening in a dielectric layer on a semiconductor substrate;

an alloy material formed on the semiconductor substrate and within the contact opening in the dielectric layer;

a continuous barrier metal formed within the contact opening in the dielectric layer, formed over and adjoining walls of the contact opening and the alloy material;

a first contact material formed over the barrier metal; and

a second contact material formed over the first contact material.

13. The conducting interface device of claim 12, wherein the alloy material includes silicon and germanium.

14. The conducting interface device of claim 12, wherein the barrier metal includes:

a layer of titanium (Ti); and

a layer of titanium nitride (TiN) coupled to the layer of titanium (Ti).

15. The conducting interface device of claim 12, wherein the alloy material is formed on the semiconductor substrate and within the contact opening by epitaxial deposition.

16. The conducting interface device of claim 12, wherein the first contact material includes a refractory metal.

17. The conducting interface device of claim 12, wherein the second contact material includes aluminum.

18. A conducting interface device comprising:

a contact opening in a dielectric layer on a semiconductor substrate;

a silicon germanium portion formed on the semiconductor substrate and within the contact opening in the dielectric layer;

a continuous barrier layer including titanium and titanium nitride formed within the contact opening in the dielectric layer, the barrier layer being formed over and adjoining walls of the contact opening and the silicon germanium portion; and

an aluminum contact material formed over the barrier layer.

19. The conducting interface device of claim 18, wherein the silicon germanium portion includes epitaxial silicon germanium.

20. The conducting interface device of claim 18, further comprising a transistor source/drain region in the semiconductor substrate wherein the contact opening opens to at least a portion of the transistor source/drain region.

21. A conducting interface device comprising:

a contact opening in a dielectric layer on a semiconductor substrate;

a silicon germanium portion formed on the semiconductor substrate and within the contact opening in the dielectric layer;

a continuous barrier layer including titanium and titanium nitride formed within the contact opening in the dielectric layer, the barrier layer being formed over and adjoining walls of the contact opening and the silicon germanium portion;

a refractory metal contact material formed over the barrier metal; and

an aluminum contact material formed over the refractory metal contact material.

22. The conducting interface device of claim 21, wherein the silicon germanium portion includes epitaxial silicon germanium.

23. The conducting interface device of claim 21, further comprising a transistor source/drain region in the semiconductor substrate wherein the contact opening opens to at least a portion of the transistor source/drain region.

24. The conducting interface device of claim 21, wherein the refractory metal contact material includes tungsten.

25. A conducting interface device comprising:

a contact opening in a dielectric layer on a semiconductor substrate;

an oxide layer formed over walls of the contact opening in the dielectric layer; and

a silicon germanium portion adjoining the semiconductor substrate and adjoining the oxide layer within the contact opening, wherein the oxide layer separates the silicon germanium portion from the dielectric layer.

26. The conducting interface device of claim 25, wherein the silicon germanium portion extends to a level below a top surface of the dielectric layer.

27. The conducting interface device of claim 25, wherein the oxide layer includes tetraethyl orthosilicate (TEOS).

28. The conducting interface device of claim 25, wherein the silicon germanium portion includes epitaxial silicon germanium.

29. The conducting interface device of claim 25, wherein the silicon germanium portion includes a silicon germanium implanted region in the semiconductor substrate.